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A 1-WATT, 8-17 GHz FET POWER AMPLIFIER

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ABSTRACT

Design and performance of a compact size 1-Watt, 8-17 GHz, 38 ± 3 dB gain FET amplifier for airborne ECM applications is described. The amplifier with a gain temperature compensation PIN diode stage and a bias regulator is packaged in 1.1 x 0.5 x 3.65 inches hermetically sealed housing.

INTRODUCTION

In ECM system applications, there are constant demands for reliable, compact size solid state amplifiers with higher output power capability and broader bandwidth coverage. Recent advances in FET device and circuit technology have made possible the achievement of octave bandwidth amplifiers with output powers of several watts in C and X-Band[1,2] and one watt from X to mid Ku-Band.[3,4] However, for the full X to Ku-Band frequency coverage, the output power is still limited to a few hundreds of milliwatts.[5] The technical difficulty is that the device transfer gain $|S_{21}|^2$ is relatively low at high frequencies.

Furthermore, for high power amplification, large gate periphery FETs have to be used. Large gate periphery FETs not only have lower device transfer gains, but they also have lower input and output impedance levels so that broadband impedance matching network design becomes a very difficult task. In this paper, we shall describe a fully integrated compact size multi-stage 8 to 17.5 GHz one watt power amplifier developed for airborne ECM system applications. Band pass filter type impedance matching networks were employed in the circuit design. Raytheon's via hole source connected power FETs[6] were used in the medium power and high power stages. The multi-stage FET amplifier with a gain temperature compensation PIN diode stage and a bias regulator is packaged in a 1.1" x 0.5" x 3.65" hermetically sealed aluminum housing. The amplifier was designed to operate over the temperature range of -54°C to +85°C and is capable of withstanding full military airborne environments. The amplifier was designed for low cost large volume production.

AMPLIFIER DESIGN

Block Diagram

The block diagram of the multi-stage amplifier chain is shown in Figure 1. The amplifier chain consists of seven low power, two medium power and one high power amplifier stages. A gain temperature compensation PIN diode stage is located in the middle of the low power section. All stages, including temperature compensation, are in a balanced configuration. The gain distribution and power budget for each amplifier stage are also shown in Figure 1. Each low power stage provides nominal gain of 5 dB, while the medium power stage and high power stage give 4.5 dB and 3 dB respectively. The PIN diode temperature compensation stage is set to -9 dB attenuation at room temperature and will vary from -2 dB at +85°C to -17 dB at -54°C. The overall amplifier is designed for a total nominal small signal gain of 38 dB.

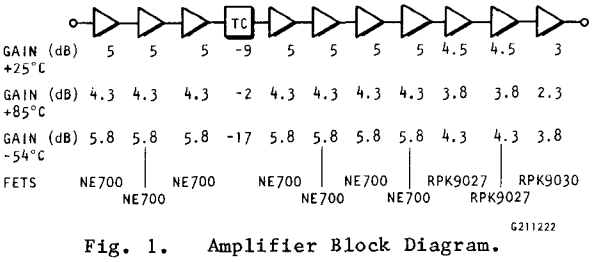

Fig. 1. Amplifier Block Diagram.

Circuit Design

Commercially available 0.5 x 300 um gate FETs (NE 700) were used in the low-power stages. Raytheon's RPK 9027 and RPK 9030, having gate peripheries of 800 um and 1600 um, were used in the medium power stage and high power stage respectively. These power FETs were fabricated with via-hole source connections for low inductance, low thermal resistance and enhanced high frequency gain and power operation. These power FETs were fabricated on vapor phase epitaxial material with active layer doping density of 2.0 x 10^{17} cm^{-3}. The RPK 9027 and RPK 9030 have output power capabilities of 0.5 watt and 1.0 watt with typical associated gains of 6.0 dB and 5.0 dB respectively, measured at 18 GHz.

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All types of devices used in the amplifier design were first mounted in a 50 ohm microstrip circuit to fully characterize their S-parameters and then device equivalent circuits were derived by curve fitting to the measured S-parameters. The equivalent circuit for the RPK 9027 FET obtained this way is shown in Figure 2. The advantage to using equivalent circuits in place of S-parameters in computer-aided circuit design is the ease with which the amplifier's sensitivity to device physical parameter variations can be studied.

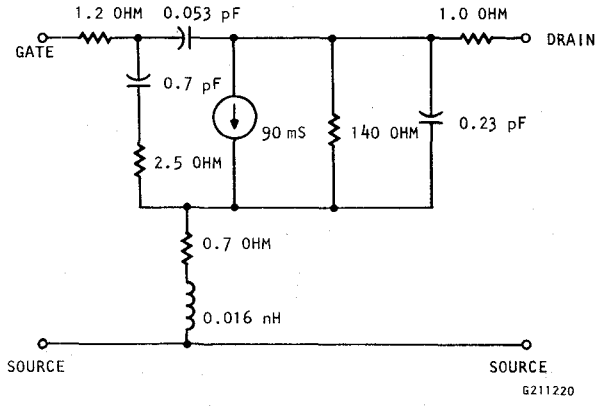

Fig. 2. FET Equivalent Circuit.

The main impedance matching networks for each amplifier stage, for both gate and drain circuits, are derived from an N = 3 bandpass filter type impedance matching network. A bandpass triple tuned impedance matching network is shown in Figure 3a. It consists of two shunt resonators and a quarter-wavelength impedance transformer.

In our study, it was found that the second resonator had only a slight effect on the amplifier response and, therefore, it was eliminated in the final circuit realization. The capacitance in the first resonator is realized by a small section of open circuited shunt stub and the inductance is realized by a 0.0007 inch gold shunt bond wire. The MIC layout of the final impedance matching network is shown in Figure 3b. A small section of transmission line "1" and a bond wire are also needed to bridge between the FET and the matching network. The length of the transmission line and the bond wire must be properly chosen for the various types of devices so that proper phasing can be obtained between each device and its matching network.

The complete amplifier impedance matching networks and a pair of 3 dB couplers for each balanced amplifier stage were fabricated on 0.015 inches thick alumina substrates and were mounted on a metal carrier. The carrier size for the low power stage is 0.25" x 0.65" and the size of the power stage is 0.32" x 0.65". Typical measured gain and power outputs of low power, and medium power and final output stages across the frequency band from 8 to 16.0 GHz are tabulated below.

STAGE	GAIN (dB)	SATURATED POWER (dBm)	POWER AT 1dB COMPRESSION PT (dBm)
Low Power NEC 700	5.5±.5	18±2	15±2
Medium Power Raytheon RPK 9027	5±1	28±1	26±1
High Power Raytheon RPK 9030	3±1	30±1	28±1

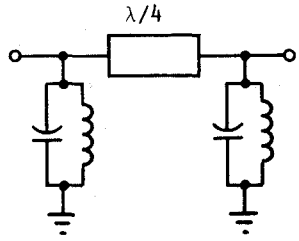

Fig. 3a. Triple Tuned Impedance Matching Network.

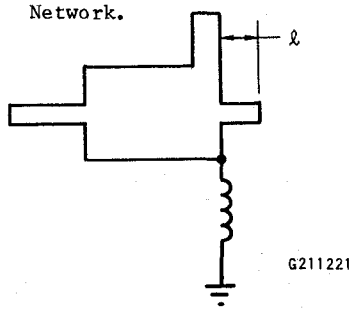

Fig. 3b. MIC Layout of Impedance Matching Network.

Amplifier Integration

The complete integrated amplifier is shown in Figure 4. Each amplifier stage was tuned and tested before mounting into the final housing. All low power stages were driven by a common +5V chip regulator located near the DC input power terminals. The temperature compensation stage with its temperature sensing driver circuit was mounted on the same size carrier as the low power stage. Each of the medium power and the high power stages contained its own regulator chip regulated at +8V. The gate bias for all power stages was derived from a -5V

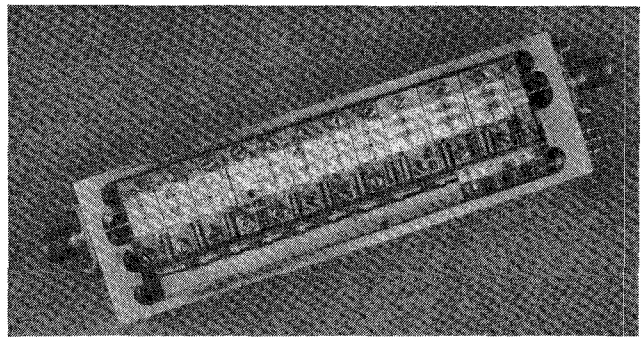

Fig. 4. Amplifier Without Top Cover.

chip regulator. The complete amplifier was packaged in a 1.1" x 0.5" x 3.65" aluminum housing. The amplifier was hermetically sealed by a laser welding technique. The amplifier was designed to meet the shock and vibration requirements of military airborne environments.

AMPLIFIER PERFORMANCE

The gain and power output response of the amplifier is shown in Figure 5; 38 ± 3 dB gain with saturated power output of 30 ±1 dBm was measured across the frequency band of 8-17 GHz. The power output at 1 dB gain compression is approximately 2 dB lower than the saturated power output. The noise figure of the amplifier is 6-8 dB and VSWR is 2.3:1 maximum. The power output variation over -54°C to +85°C temperature is shown in Figure 6. Variation of ± 1 dB was measured at the temperature extremes. The total DC current drain is 1.5 amps from +12V supply and 10 mA from -12V supply.

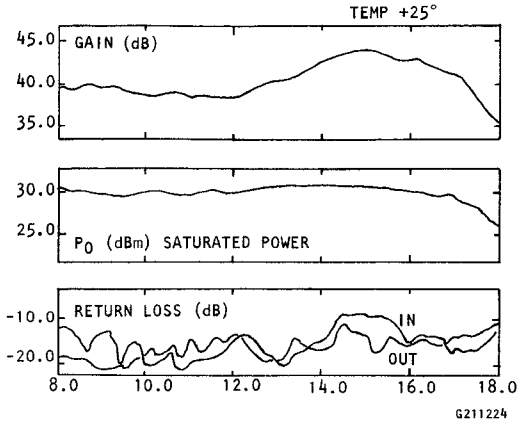

Fig. 5. Gain, Power Output, and VSWR of the Amplifier.

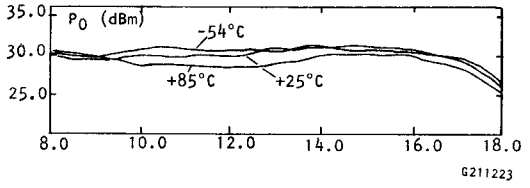

Fig. 6. Power Performance of the Amplifier Over Temperature.

CONCLUSION

A compact size 8-17 GHz FET power amplifier was developed with a power output capability of 30 ± 1 dB. The amplifier was designed for large volume, low cost production. It is suitable for many applications either in existing ECM systems as a TWTA replacement or in newly designed systems as a medium power amplifier.

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